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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,288	09/12/2003	Michael A. Duncan	CHA920030019US1	7423

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EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/661,288	DUNCAN ET AL.	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-17 and 19-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-17 and 19-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's amendment and arguments, filed 10/12/2006, with respect to the 35 U.S.C. §112 rejection of claims 12-14 have been fully considered and are persuasive. The U.S.C. §112 rejection of claims 12-14 has been withdrawn.

2. Applicant's arguments regarding the prior art, filed 10/12/2006, have been fully considered but they are not persuasive. Examiner's rebuttal is detailed below.

Issue 1

3. Applicant argues that real-time data cannot be "low latency" as newly amended into the independent claims.

Examiner contends that "low latency" is a relative term, even more so in the independent claims that do not recite 'real-time' giving nothing to compare what is meant by "low latency". Even if these particular claims expressly indicated some form of 'real-time' communications, Examiner does not agree that a skilled artisan in the art would rule out real-time communications involves low latency. In fact, it is physically impossible to have something with zero latency. Real-time devices merely have low enough latency such that any delay in operation is not perceivable to the user. Latency is still inherent to the real-time device. Given that there is indication of the degree of how low the latency is in the application, one cannot exclude real-time communications. This is further supported by extrinsic evidence to US Pat. No. 6,366,989 to Keskar et al. who expressly discloses real time data in multimedia applications having low latency *(Column 1, lines 35-30).*

Issue 2

4. Applicant argues the limitation "external devices" connotes devices that are located away from the computer system instead of within the computer system, to the extent that they are located up to 30 feet away.

Examiner contends that the claim language itself does not require this narrow interpretation. Applicant appears to associate "external device" with a 'remote device'. Nowhere in the claim language recites or alludes to the external device actually being remote from the computer system. Examiner further contends an "external device" can be construed to be an external peripheral card, one that is removable from the slots within the computer system. From the claim language, the recited "peripheral interface device" is located/adapted within the computer system and the external devices interface the peripheral interface device. Clearly within the scope of the claims, the "external devices" can be physical devices that can interface and is not already integrated with the peripheral interface device. Therefore, the physical cards that plug into the slots of the multimedia device interfaces (Fig. 1, elements 142-146), the multimedia device interfaces themselves being resident on a motherboard that is equated to the peripheral interface device, are the external devices.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1,12,13,17,28,29 and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. The term "low latency" in claims 1,12,13,17,28,29 and 33 is a relative term which renders the claim indefinite. The term "low latency" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Examiner will assume low latency to be the speed for operations of real or non-real time operations. All respective dependent claims are rejected due to the rejected base claim.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3-17 and 19-34 are rejected under 35 USC 103(a) as being unpatentable over US Pat. No. 5,809,261 to Lambrecht in view of US Pat. Pub. No. 2005/0038947 to Lueck et al. (Lueck).

10. Per claims 17, Lambrecht discloses a computer system *(Fig. 1)* comprising a processing unit *(Fig. 1, element 102)*; a memory *(Fig. 1, element 110)*; an I/O bus coupled to the processing unit and memory *(Fig. 1, element 120 and 130)*; and a peripheral interface device/interface host motherboard card *(Fig. 1, elements 142, 144 and 146 are all construed to be the singular peripheral interface device since all of them each indeed interfaces to external peripheral devices. To be more exacting, the motherboard backplane under which the multimedia devices sit, is the "peripheral interface device", the backplane accommodating multiple multimedia device ports/connectors, elements 142, 144 and 146; the backplane is construed to be one large interface card, adaptable to accommodate multiple daughter cards)* which provides a communication interface for a plurality of external devices *(elements 142-146 are external device interfaces; Fig. 4, element 132 show that the interface is slots; Column 13, lines 58+ disclose examples of different external peripheral multimedia devices)*, wherein the peripheral device includes: a plurality of transfer control logic modules TCL *(Figs. 2, 11, 8 show details of each module, elements 142-146 that allows an external device to attach to the host)*, wherein each TCL module includes an interface for a dedicated external device *(slots shown in Fig. 4 are the interfaces, interfacing the digital logic shown in Fig. 8)*, wherein the multiple TCL modules can communicate in parallel with their external devices with low latency *(Fig. 5, PCI and*

multimedia bus are inherently parallel standards, Lambrecht is directed towards real time multimedia, see abstract, requiring high throughput); and a dual port memory DPM device *(Fig. 15, element 160; Column 20, lines 60+, "...multimedia memory 160 is preferably dual ported memory..."; real time operations work at very low latencies)* that is in communication with the I/O bus *(Fig. 15 clearly shows communication with both the multimedia and PCI buses)*, wherein the DPM device can selectively communicate data with each of the plurality of TCL modules *(dual port memory 160 is shared by all multimedia devices, elements 142-146)*. Lambrecht further discloses TCL modules *(142-146)* communicate with DPM requiring the use of arbitration *(Column 9, lines 28-35 disclose "...the transferring device acts as a PCI bus master for setting up the multimedia transfer...It is noted that the transferring device may first be required to arbitrate for control of the PCI bus 120. Once the transfer has been set up on the PCI bus 120 in step 302, then in step 304, then the transferring device performs the data transfer on the multimedia bus 130 to the receiving or target device.")*.

Lambrecht does not disclose expressly the arbitration between the DPM device and TCL modules being performed in a round-robin fashion.

Lueck discloses a similar PCI communications bus structure to the one by Lambrecht (Fig. 2), particularly a plurality of card devices *(Fig. 2, elements 230, 234 and 238)* sharing a PCI bus *(Fig. 2, element 228)*, wherein an arbiter *(Fig. 2, element 226)* arbitrates for the bus for each of the PCI devices. Lueck expressly discloses, in paragraph 4, *round-robin arbitration to be typical to PCI architecture*. Paragraph 4 of Lueck states, "...In a PCI bus architecture, the bus arbiter utilizes a round-robin

arbitration which is "fair" to all devices on the bus. Once the device on the bus has received a grant to use the bus, it can hold on to the bus until its transaction is complete...".

Lambrecht and Lueck are analogous art because they are from the same field of endeavor in PCI arbitration where there exists a plurality of competing devices that share a PCI bus and having an arbiter that grants the devices access to the bus based on arbitration.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use round-robin arbitration.

The suggestion/motivation for doing so would have been it is typical and well-known to use round robin in PCI as stated by Lueck. Furthermore, the devices in Lambrecht that share the bus do not have a priority order *per se*, e.g., all are real-time devices where any particular one does not have priority over the other, so round-robin techniques are an obvious choice.

Therefore, it would have been obvious to combine Lambrecht with Lueck for the benefit of using well-known and typical PCI arbitration round-robin means to grant access to a plurality of non-priority devices.

11. Per claims 1 and 33, claim 17 is substantially similar and therefore the rejection is applied accordingly.

12. Per claims 3-9,13,14, 19-25,29,30 and 34 Lambrecht combined with Lueck, disclose claims 1,17 and 33, Lambrecht further disclosing having specific control channel interface for each multimedia interface/device *(Fig. 8, element 526 interfaces*

control bus, Fig. 7, element 502) where read/writes to the host multimedia/PCI bus are handled via this control bus and the transactions over the bus are operated via various types of commands such as interrupts, status commands, etc *(Column 13, lines 30+ disclose the control interface and control bus 526 interrupts, synchronizes, relays status commands, etc.)*.

13. Per claims 15,16 and 31, 32, Lambrecht combined with Lueck disclose claims 1 and 17, wherein Lambrecht further discloses the peripheral interface device is a PCI adapter card *(as stated, the peripheral interface device is the backplane having slots that adapt to peripheral PCI cards or multimedia cards; the peripheral interface device is thus construed, itself, to be a PCI adapter card, able to accommodate multiple daughter PCI cards)*.

14. Per claims 10,12 and 26,28, Lambrecht combined with Lueck disclose claims 1 and 17, Lambrecht further discloses the dual port multimedia memory *(Fig. 15, element 160)* has memory regions that stores writes and reads to the external device *(Column 22, lines 15-20, "...multimedia devices 142C-146C can gain control of the real-time bus 130 and access the multimedia memory 160 to retrieve desired code and data..."; Column 21, lines 55-60, "...multimedia devices 142C-146C also communicate data between each other and the multimedia memory 160 using the real-time bus or multimedia bus 130...". Note the claim language does not dictate that each device has its own separate region in the multimedia memory, e.g., on can view the multimedia memory 160 as a memory pool that is overwritten each time a external device writes to it)*.

15. Per claims 11 and 27, Lambrecht combined with Lueck disclose claims 1 and 17, Lambrecht further disclosing each TCL module includes a control register for controlling data transfers between the computer system and the TCL module *(Fig. 14, elements 712-716 show registers for controlling data between system and each TCL modules 142-146)*.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patents and patent related publications are cited in the Notice of References Cited (Form PTO-892) attached to this action to further show the state of the art with respect to real-time data and low latency.

US Pat. No. 6,366,989 to Keskar et al. discloses a PCI based system that implements multimedia processing in real time, where real time is clearly stated as having low latency *(Column 1, lines 25-30)*.

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ASC
12/07/2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER

12/7/06